DVB-S2 Receiver ASIC (ECC3100)

Digital Satellite Communications Receiver Chip

The Viasat receiver chip is an innovative satellite communications device that leverages the unprecedented power and bandwidth efficiencies of the DVB-S2 standard.

Our unique design experience merges advanced Adaptive Coding and Modulation (ACM), Forward Error Correction (FEC), and Application Specific Integrated Circuit (ASIC) technology to create the premier solution for next generation satellite communication systems.

A wide range of symbol rates and data formats are supported by the chip, including MPEG transport streams, generic data streams and ULE packets. It may be embedded in various types of broadband via satellite equipment such as SCPC modems and VSATs as well as receive-only and hybrid terminals. It also supports the interactive services modes defined in the DVB-S2 standard that allow network operators to provide the benefits of ACM to their subscribers.

The receiver ASIC features a host of unique attributes making it the premier choice for your design.

DVB-S2 RECEIVER ASIC 3100 AT-A-GLANCE

- DVB-S2 standard compliant
- Symbol rates from 100 KSps to 50 MSym/sec
- QPSK, 8 PSK, and 16 APSK demodulation
- LDPC/BCH decoding with demodulator bypass mode (decoder only)
- Constant (CCM), Variable (VCM) and Adaptive
- (ACM) Coding and Modulation
- Low implementation loss achieves near shannon-limit performance

Typical Applications

- High-performance professional Integrated Receiver Decoders (IRDs)
- Ruggedized/MIL-SPEC broadband VSAT modems with ACM capabilities
- Digital Satellite News Gathering (DSNG)
- Secure high bandwidth/high bitrate video and data links

Key Features

- 100 KSps symbol rate/FEC 1/4
- Complimentary multistream extraction and Input Stream Identifier (ISI) filtering
- 0° to 70° C operating ambient temperature range
- TS bypass mode
- Capable of implementing NSA approved Joint IP Modem TRANSEC

Target Applications

- Ultra-low bandwidth satellite radio broadcasting and distribution digital signage over satellite
- Next generation IRDs requiring simultaneous decode/demodulation of multiple transport streams
- Ruggedized DVB-S2 receiver, SCPC modems and VSATs
- High level encryption DVB-S2 satellite test and measurement
- Military's Global Broadcast Service (GBS) and Joint IP Modems networks

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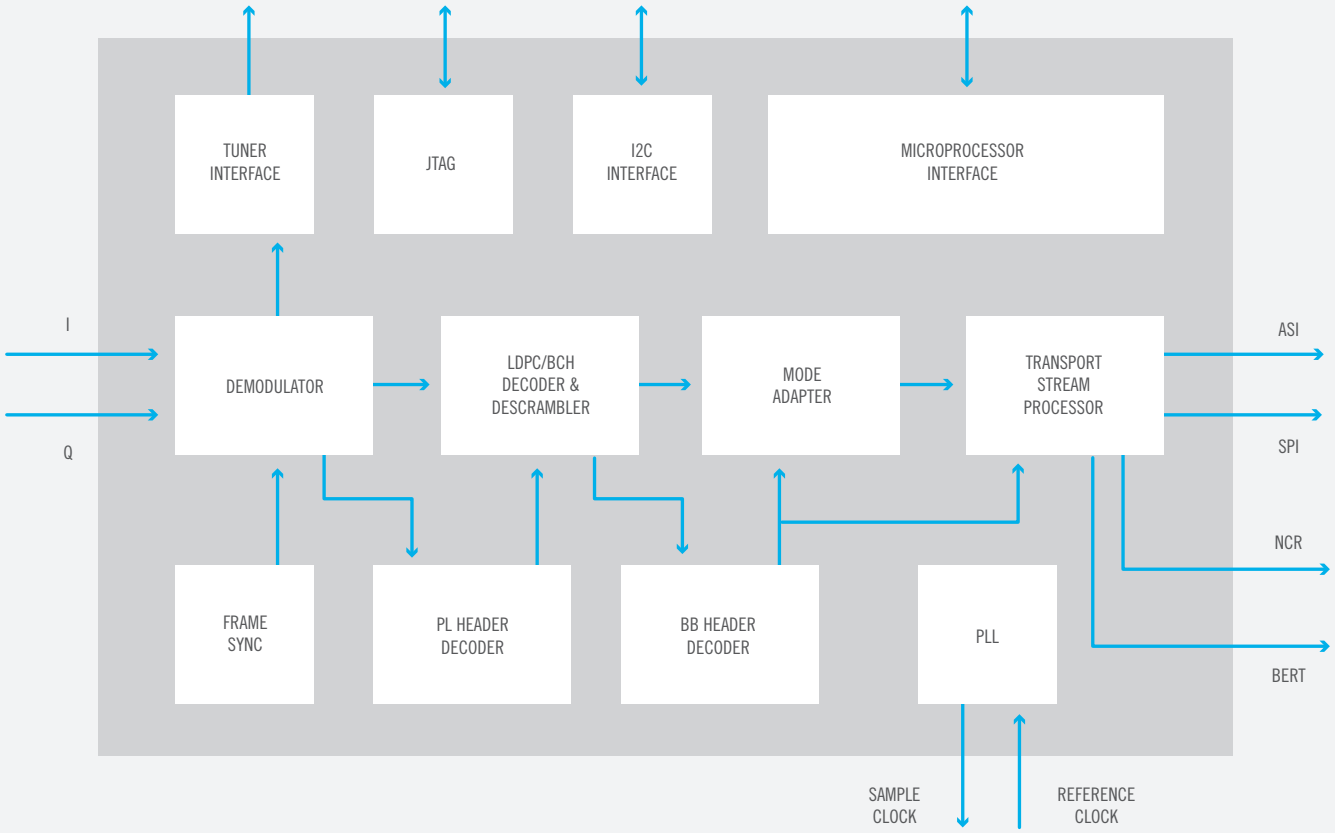
RECEIVER BLOCK DIAGRAM



The distinctive architecture of the receiver chip enables vendors of interactive, broadcast and mobile satellite communications equipment to deliver the most cost-effective, high-performance, leading-edge products to the consumer, enterprise and government markets.

Demodulation, decoding and transport stream processing functions are integrated by the chip, as defined in the DVB-S2 standard, into a single ASIC. It clocks the A/D converter at rates up to 135MHz and accepts 8-bit, offset binary or two's complement, digital I-Q samples. The maximum symbol rate of the receiver chip is equal to 0.375 times the sample clock rate (e.g. 45 MSps for a 120 MHz clock).

MPEG transport streams and generic data streams can be processed by the chip. It can also extract ULE packets encapsulated within MPEG frames and output them via the microprocessor's local bus interface. Data can be filtered according to either a stream identifier in the DVB-S2 baseband header or a set of PIDs. The demultiplexed data is then output via SPI or ASI.

The receiver chip facilitates development of next generation one-way and two-way DVB-S2 terminals. It is implemented in a well integrated, cost-effective 256-pin LQFP package with a 28 x 28 mm^2 footprint and with a 14 x 14 mm^2 exposed pad.

Bits per symbol ratios indicate the total number of bits, including DVB-S2 frame overhead divided by the number of modulated symbols. Required Es/No includes implementation losses in L-band loop back, for modulator, frequency upconverter, tuner, and DVB-S2 receiver chip.

KEY BENEFITS

Improves Link Performance (Relative to the DVB-S Standard)

- 35% more throughput or equivalently 25% less bandwidth
- Smaller receive antenna or lower downlink EIRP required
- ACM doubles system capacity under typical conditions
- 2.8 dB more link margin on average

Boosts Link Availability

- Dynamic SNR range greater than 14 dB
- ACM counters rain fades with over 20 modulation and coding choices
- Maximum likelihood phase tracking provides excellent phase noise performance
- Usable satellite transponder footprint extended to geographic edge-of-coverage

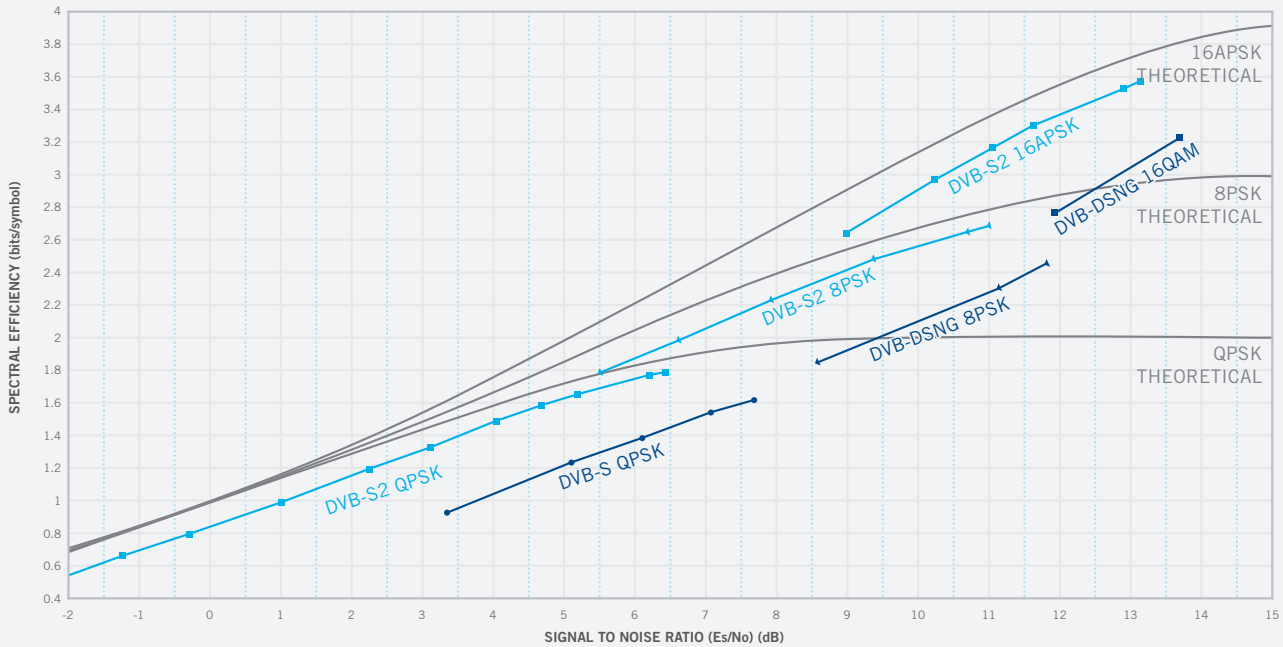
Reduces Time-to-Design and Time-to-Market

- System-on-a-chip architecture facilitates rapid, low-cost terminal development
- Flexible evaluation platform, easy-to-configure software and technical support

Targets Professional Satcom Applications

- Interoperable with commercial-off-the-shelf DVB-S2 modulators
- Open standard implementation suitable for multi-vendor environment

DVB-S2 PERFORMANCE CURVES



SPECIFICATIONS

DVB-S2 CONFIGURATION OPTIONS

- Matched filtering with 0.20, 0.25 or 0.35 roll-off factor
- Normal frames of 64,800 bits or short frames of 16,800 bits
- Pilot tone insertion
- Spectrum inversion

PACKET AND STREAM PROCESSING CAPABILITIES

- MPEG transport streams, generic data streams or ULE packets
- Filtering on stream identifiers in DVB-S2 baseband headers
- Filtering on PIDs in MPEG transport streams
- Transport layer bypass mode (outputs full baseband frames)
- ULE extraction via local bus interface

DATA AND DIAGNOSTIC INTERFACES

- MPEG SPI/ASI (8-bit)
- Local bus interface configurable for various microprocessors (16-bit)
- BERT interface
- JTAG boundary scan

CONTROL AND CLOCK INTERFACES

- I2C interface configuration
- Tuner AGC interface (pulse-width modulation)
- Internal PLL accepts external clock reference
- NCR interface distributes clock recovered from DVB-S2 carrier signal

DVB-S2 RECEIVER PERFORMANCE (64,800 b Frames Measured at 30 MSps)

MOD	LDPC CODE IDENTIFIER	BW EFFICIENCY	Es/No [dB] (QEF)	Eb/No [dB] (QEF)
QPSK	1/4	0.49	-1.6	1.5
QPSK	1/3	0.66	-0.9	0.9
QPSK	2/5	0.79	0.1	1.1
QPSK	1/2	0.99	1.3	1.3
QPSK	3/5	1.19	2.7	2.0
QPSK	2/3	1.32	3.3	2.1
QPSK	3/4	1.49	4.2	2.5
QPSK	4/5	1.59	4.9	2.9
QPSK	5/6	1.65	5.4	3.2
QPSK	8/9	1.77	6.4	3.9
QPSK	9/10	1.79	6.6	4.1
8PSK	3/5	1.78	5.9	3.4
8PSK	2/3	1.98	6.9	3.9
8PSK	3/4	2.23	8.2	4.7
8PSK	5/6	2.48	9.6	5.7
8PSK	8/9	2.65	10.9	6.7
8PSK	9/10	2.68	11.2	6.9
16APSK	2/3	2.64	9.3	5.1
16APSK	3/4	2.97	10.5	5.8
16APSK	4/5	3.17	11.4	6.4
16APSK	5/6	3.30	11.9	6.7
16APSK	8/9	3.52	13.1	7.6
16APSK	9/10	3.57	13.3	7.8

CONTACT

SALES
TEL +1 216 706 7800 **EMAIL** asics@viasat.com **WEB** www.viasat.com/advanced-technology