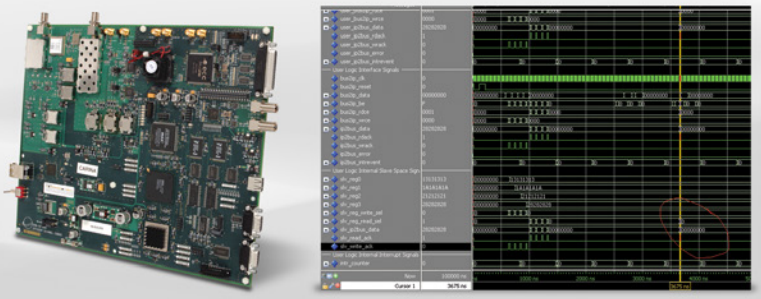
IP Cores Summary

Advanced FEC Cores for Wireless and Wired Application

Viasat specializes in communication and Forward Error Correcting (FEC) IP cores. These IP cores were developed for advanced satellite and wireless communication systems with high standard requirements.



Our IP cores are proven in ASICs and FPGAs. The FEC cores were initially developed for satellite and video applications. Our flexible underlying architecture is configurable for WiMAX, 3GPP, GPON, and DOCSIS applications. There are several configurations within each FEC category that can be optimized for specific applications.

RS (REED SOLOMON)

RS codes form a large class of powerful non-binary cyclic codes. The non-binary symbol based nature makes them suitable for correcting correlated error events. These codes are used as component codes for building more powerful codes like RS-TPCs or Reed-Solomon Product (RSP) and also as an error floor removal tool in concatenated codes.

Applications WiMax (802.16), DOCSIS, GPON

TPC (TURBO PRODUCT CODES)

TPCs are serially concatenated BCH codes with row/column interleaving between the inner and outer code. This structure coupled with iterative soft-decision decoding results in error-correction performance close to the Shannon limit. TPCs are particularly powerful at high code rates.

Applications WiMax (802.16), CDMA2000, GPON

CTC (CONVOLUTIONAL TURBO CODES)

CTCs use highly powerful iterative decoding to achieve performance close to coding theory limits. They employ serial or parallel concatenated convolution code with pseudo-random interleaving between the inner and outer code. CTCs perform extremely well at lower code rates and have been used in a variety of tele-communication standards including DVB-RCS.

Applications WiMax (802.16), WCDMA, CDMA2000, CCSDS

BCH (BOSE-CHAUDHURI-HOCQUENGHEM)

BCH codes form a large class of powerful random error correcting cyclic codes. These codes are used as component codes for building more powerful codes and as an error floor removal tool.

Applications Video Broadcasting, DVB-S2, memory controllers

LDPC (LOW DENSITY PARITY CODES)

LDPC is a powerful FEC option that is defined by very sparse parity check matrices. LDPC designs allow for parallel iterative decoder processing which can be implemented in hardware-friendly fashion while maintaining excellent performance close to the Shannon limit.

Applications WiMax mobile, DVB-S2

Additional IP cores available for communications system

- Filters FIR, FFT and matched
- Complete demodulators—OFDM, and DVB-S/S2 and
- Spread spectrum technologies—DSSS and FHSS

CONTACT

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